AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1, 2, 4, 12, 14, and 17 as shown below.

This claim list replaces all prior claim lists in the application.

1. (Currently Amended) A gallium nitride-based III-V group compound semiconductor device comprising:

a gallium nitride-based semiconductor layer; and

a p-type ohmic electrode layer formed on the gallium nitride-based semiconductor layer,

wherein the p-type ohmic electrode layer comprises a contact metal layer, a reflective metal layer, and a diffusion barrier layer, the reflective metal layer being disposed between the contact metal layer and the diffusion barrier layer and being in direct contact with both the contact metal layer and the diffusion barrier layer,

wherein the p-type ohmic electrode layer further comprises at least one bonding metal layer, the bonding metal layer comprising the same material as that of the contact metal layer.

2. (Currently Amended) The semiconductor device according to claim 1, wherein the contact metal layer comprises Ni ~~p-type ohmic electrode layer further comprises at least one bonding metal layer~~.

3. (Previously Presented) The semiconductor device according to claim 2, wherein the p-type ohmic electrode layer is formed by sequentially laminating the contact metal layer, the reflective metal layer, the diffusion barrier layer, and the bonding metal layer.

4. (Currently Amended) The semiconductor device according to any one of claims 1 or [[to]] 3, wherein the contact metal layer further comprises at least one of Ni, [[Ir,]]Pt, Pd, Au, Ti, Ru, W, Ta, V, Co, Os, Re, and Rh.

5. (Previously Presented) The semiconductor device according to any one of claims 1 to 3, wherein the reflective metal layer comprises at least one of Al and Ag.

6. (Previously Presented) The semiconductor device according to any one of claims 1 to 3, wherein the diffusion barrier layer comprises at least one of Ru, Ir, Re, Rh, Os, V, Ta, W, ITO (Indium Tin Oxide), IZO (Indium Zinc oxide), RuO_2, VO_2, MgO, IrO_2, ReO_2, RhO_2, OsO_2, Ta_2O_3, and WO_2.

7. (Previously Presented) The semiconductor device according to claim 2 or 3, wherein the bonding metal layer comprises first and second bonding metal layers, said first bonding metal layer comprising at least one of Ni, Cr, Ti, Pd, Ru, Ir, Rh, Re, Os, V, and Ta, said second bonding metal layer comprising at least one of Au, Pd, and Pt.

8-11. (Canceled)

12. (Currently Amended) The semiconductor device according to claim 1, wherein the contact metal layer comprises a first layer and a second layer, and

wherein the first layer comprises one of Ni, [[Ir,]]Pt, Pd, Au, Ti, Ru, W, Ta, V, Co, Os, Re, and Rh, and the second layer comprises ~~one of Ni, Ir, Pt, Pd, Au, Ti, Ru, W, Ta, V, Co, Os, Re, and Rh, and the first layer and the second layer do not comprise the same material~~.

13. (Previously Presented) The semiconductor device according to claim 12, wherein the p-type ohmic electrode layer further comprises at least one bonding metal layer disposed on the diffusion barrier layer, the diffusion barrier layer being disposed between the reflective layer and the at least one bonding metal layer.

14. (Currently Amended) The semiconductor device according to claim 13, wherein the contact metal layer further comprises a third layer, and wherein the first layer [[is]]comprises a Ni layer~~, the second layer is an Ir layer,~~ and the third layer [[is]]comprises a Pt layer, and

wherein the at least one bonding metal layer comprises a first bonding metal layer and a second bonding metal layer, the first bonding metal layer comprising at least one of Ni, Cr, Ti, Pd, Ru, Ir, Rh, Re, Os, V, and Ta, and the second bonding metal layer comprising at least one of Au, Pd, and Pt.

15. (Previously Presented) The semiconductor device according to claim 14, wherein the contact metal layer has a thickness in the range of 5 to 500 Å, the reflective layer has a thickness in the range of 100 to 9,000 Å, the diffusion barrier layer has a thickness in the range of 50 to 1,000 Å, the first bonding metal layer has a thickness in the range of 100 to 3,000 Å, and the second bonding metal layer has a thickness in the range of 100 to 9,000 Å.

16. (Previously Presented) The semiconductor device according to claim 15, wherein the thickness of the contact metal layer does not exceed 200 Å, the thickness of the reflective layer is in the range of 1,000 to 2,000 Å, the thickness of the diffusion barrier layer is in the range of 100 to 800 Å, the thickness of the first bonding metal layer does not exceed 1,000 Å, and the thickness of the second bonding metal layer does not exceed 1,000 Å.

17. (Currently Amended) The semiconductor device according to claim 1, wherein:

the p-type ohmic electrode layer further comprises a first bonding metal layer and a second bonding metal layer;

the contact metal layer is disposed directly on the gallium nitride-based semiconductor layer and further comprises a Ni layer~~, an Ir layer,~~ and a Pt layer;

the reflective layer is disposed directly on the contact metal layer and comprises an Ag layer;

the diffusion barrier layer is disposed directly on the reflective layer and comprises a Ru layer;

the first bonding metal layer is disposed directly on the diffusion barrier layer and comprises a Ni layer; and

the second bonding metal layer is disposed directly on the first bonding metal layer and comprises an Au layer.